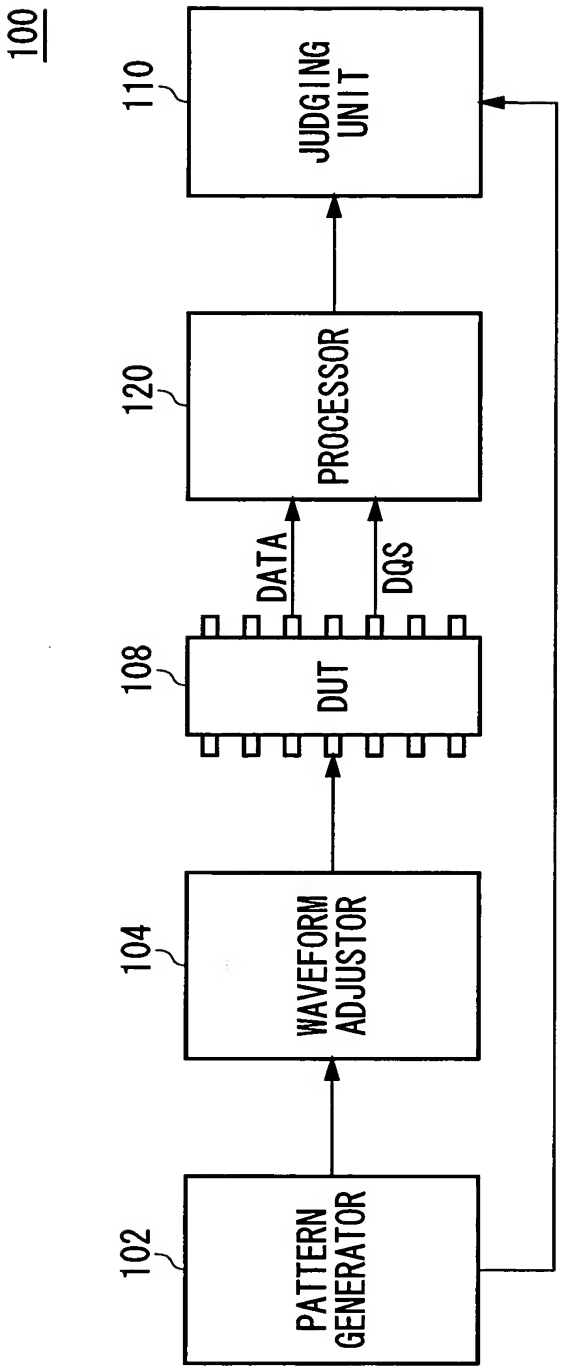
100
110
JUDGING UNIT
120
PROCESSOR
DATA
DQS
108
DUT
104
WAVEFORM ADJUSTOR
102
PATTERN GENERATOR

FIG. 1

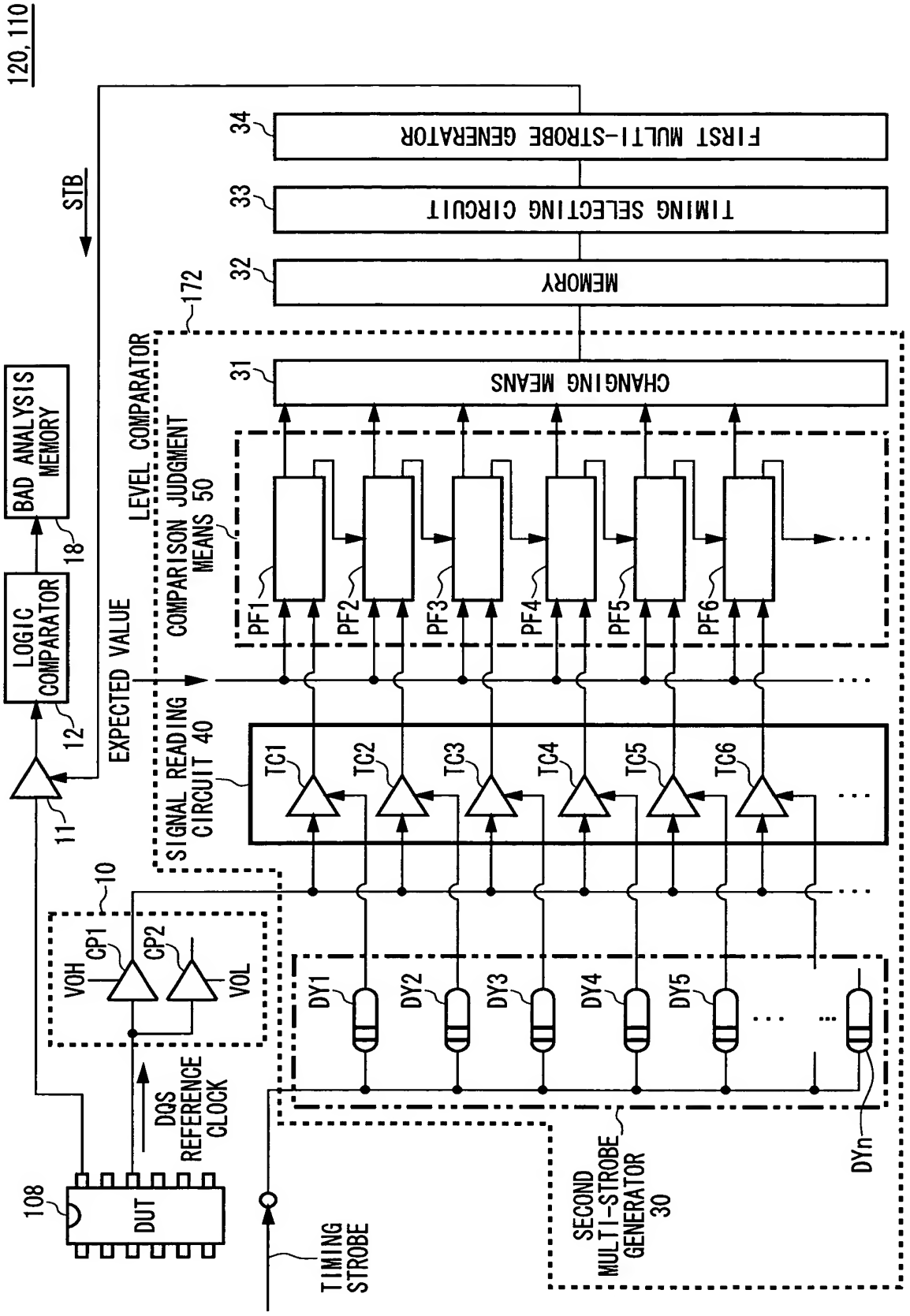
120,110
STB
34
FIRST MULTI-STROBE GENERATOR
33
TIMING SELECTING CIRCUIT
32
MEMORY
172
31
CHANGING MEANS
LEVEL COMPARATOR
COMPARISON JUDGMENT MEANS 50
PF1
PF2
PF3
PF4
PF5
PF6
BAD ANALYSIS MEMORY
18
LOGIC COMPARATOR
12
EXPECTED VALUE
SIGNAL READING CIRCUIT 40
TC1
TC2
TC3
TC4
TC5
TC6
11
10
VOH
CP1
CP2
VOL
DQS REFERENCE CLOCK
DY1
DY2
DY3
DY4
DY5
DYn
SECOND MULTI-STROBE GENERATOR 30
108
DUT
TIMING STROBE

FIG. 2

FIG. 3A

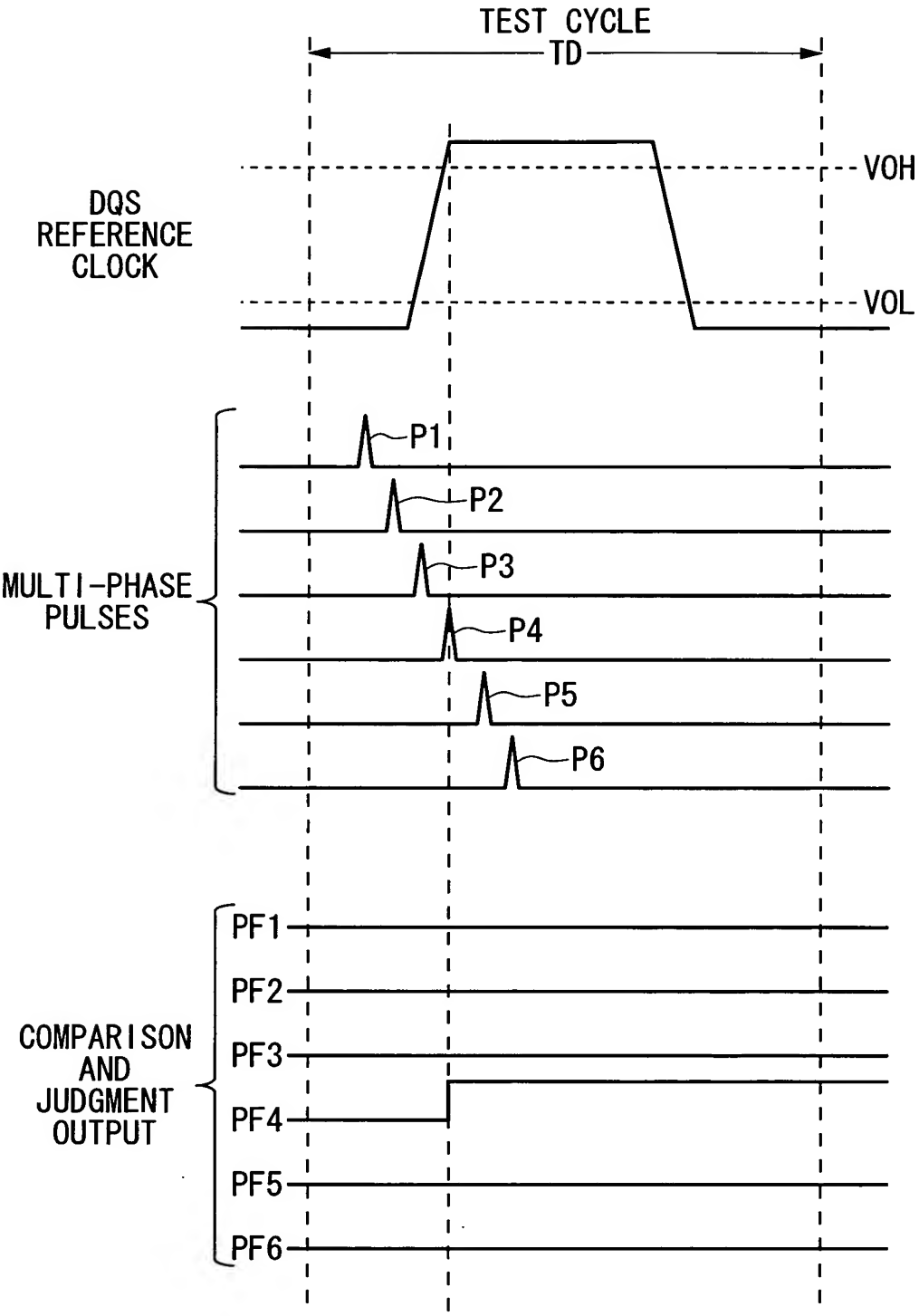

FIG. 3B

FIG. 3C

FIG. 4A

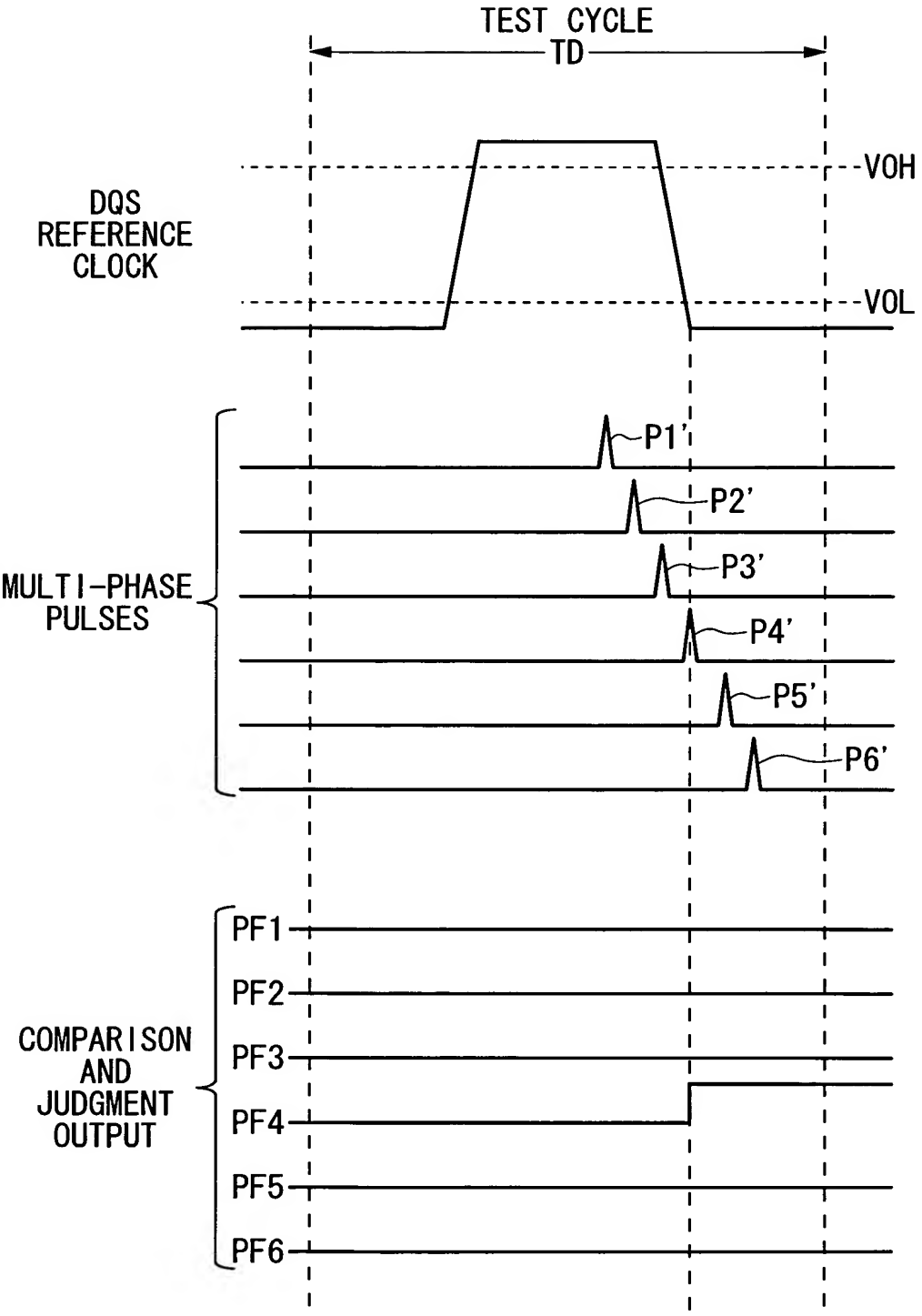

FIG. 4B

FIG. 4C

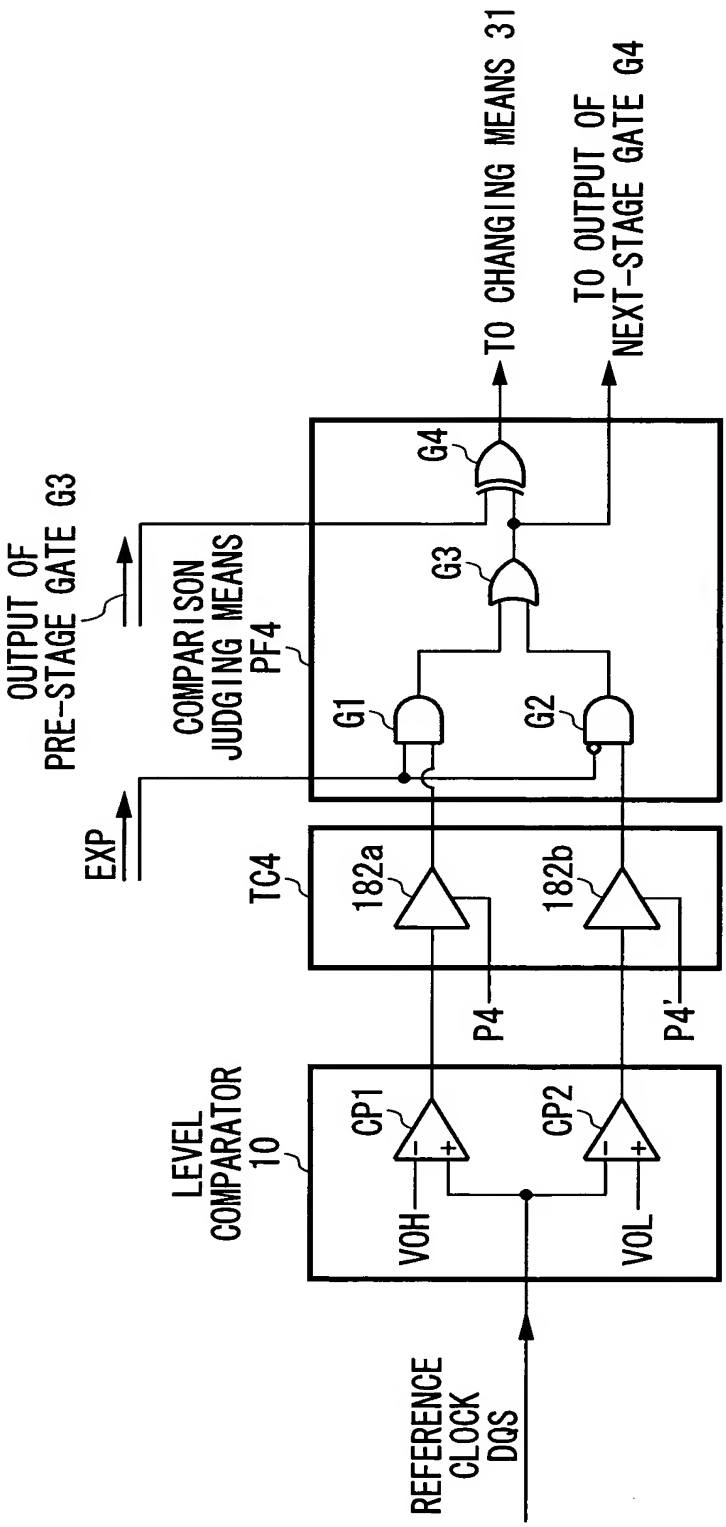
REFERENCE CLOCK DQS
LEVEL COMPARATOR 10
CP1
CP2
VOH
VOL
P4
P4'
TC4
182a
182b
EXP
OUTPUT OF PRE-STAGE GATE G3
COMPARISON JUDGING MEANS PF4
G1
G2
G3
G4
TO CHANGING MEANS 31
TO OUTPUT OF NEXT-STAGE GATE G4

FIG. 5

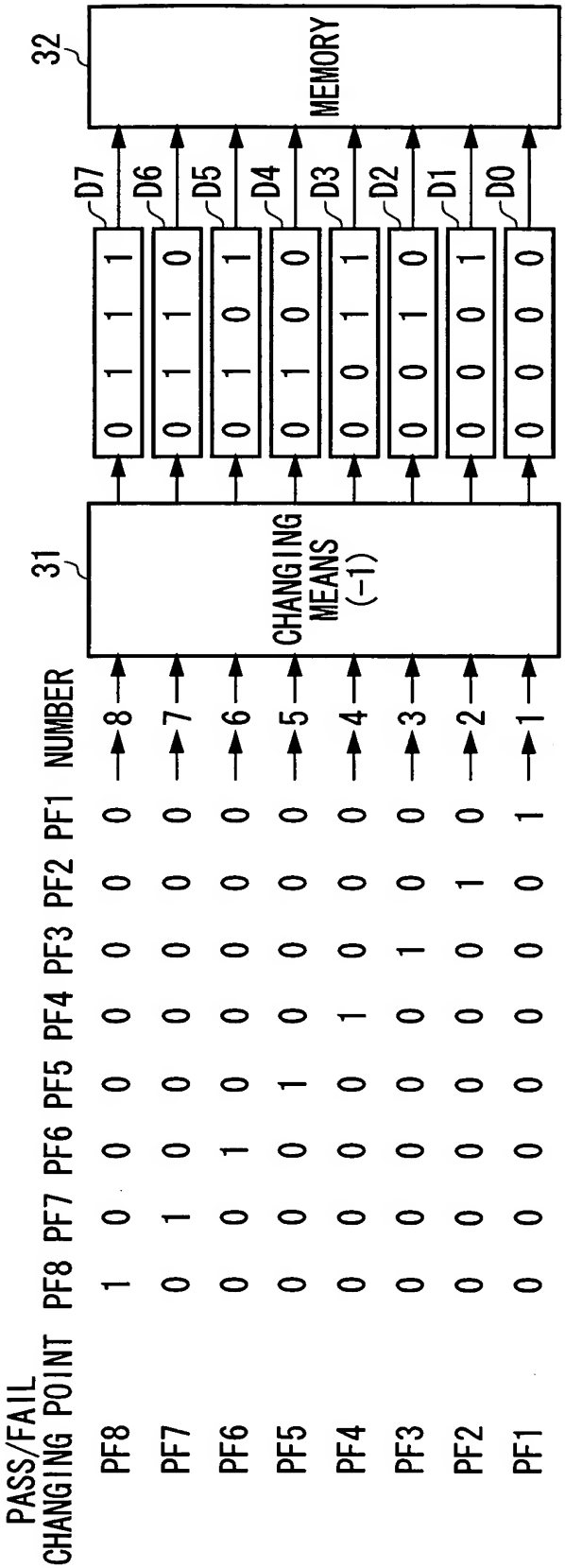
PASS/FAIL
CHANGING POINT
PF8
PF7
PF6
PF5
PF4
PF3
PF2
PF1
NUMBER
8
7
6
5
4
3
2
1
31
CHANGING MEANS (-1)
D7
D6
D5
D4
D3
D2
D1
D0
32
MEMORY

FIG. 6

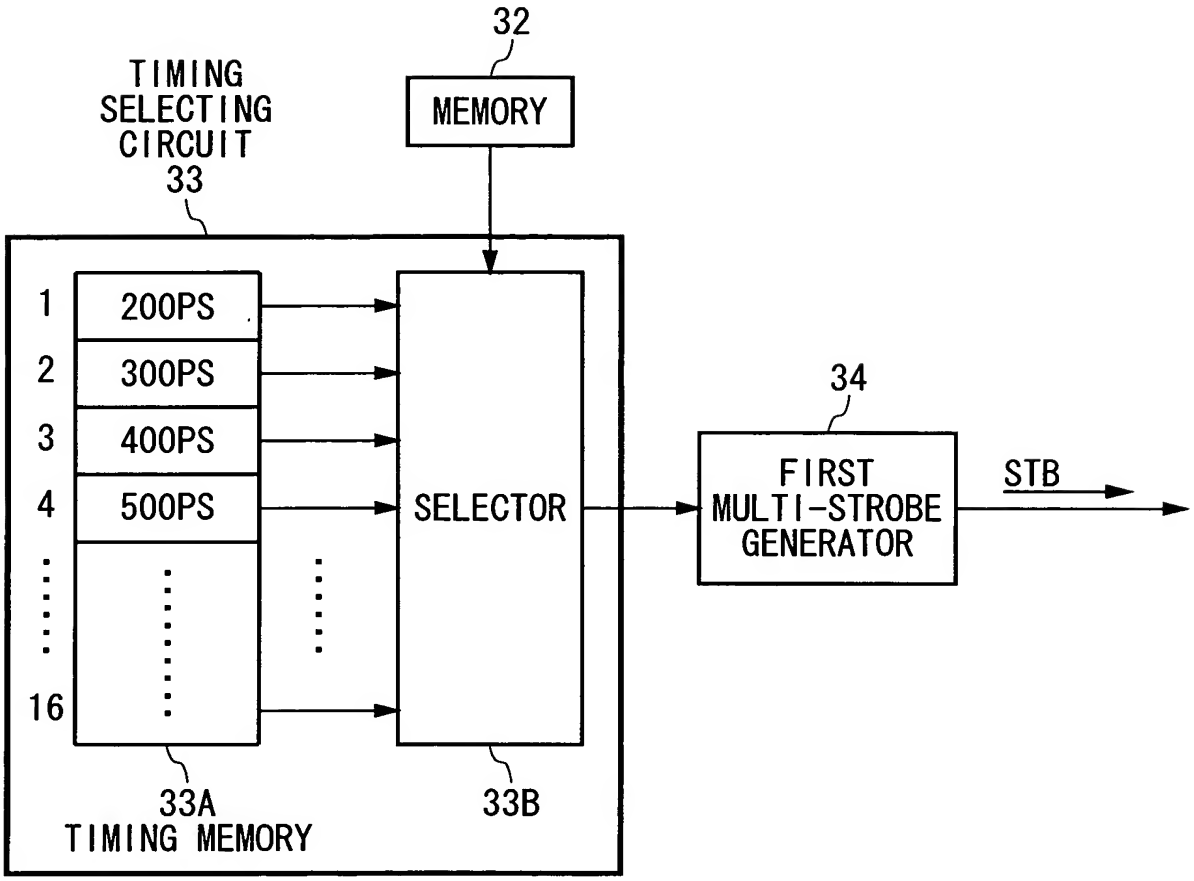
32
TIMING
SELECTING
CIRCUIT
33
MEMORY
1
2
3
4
16
200PS
300PS
400PS
500PS
SELECTOR
34
FIRST
MULTI-STROBE
GENERATOR
STB
33A
TIMING MEMORY
33B

FIG. 7

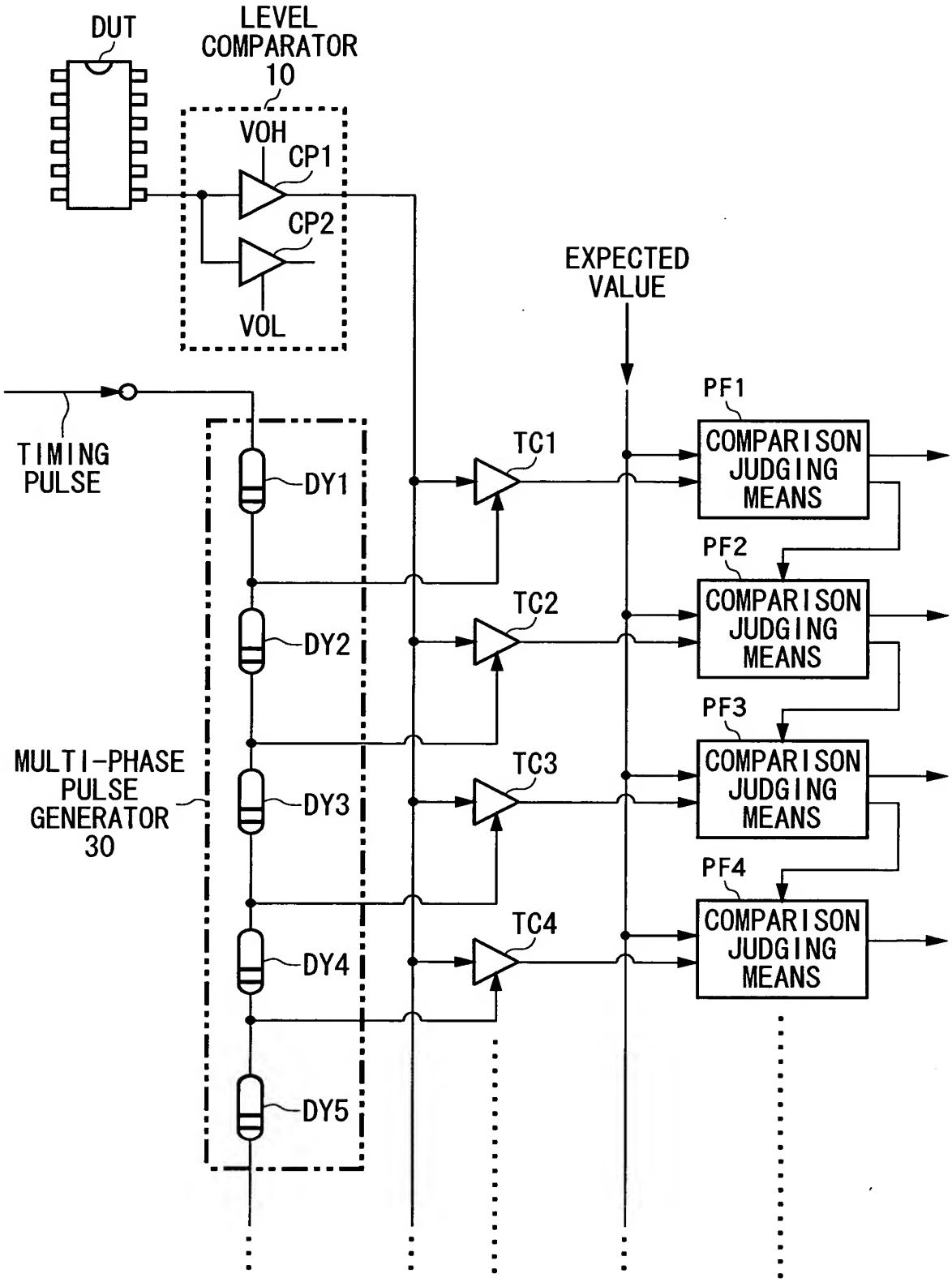
DUT
LEVEL COMPARATOR 10
VOH
CP1
CP2
VOL
EXPECTED VALUE
TIMING PULSE
MULTI-PHASE PULSE GENERATOR 30
DY1
DY2
DY3
DY4
DY5
TC1
TC2
TC3
TC4
PF1
PF2
PF3
PF4
COMPARISON JUDGING MEANS
COMPARISON JUDGING MEANS
COMPARISON JUDGING MEANS
COMPARISON JUDGING MEANS

FIG. 8

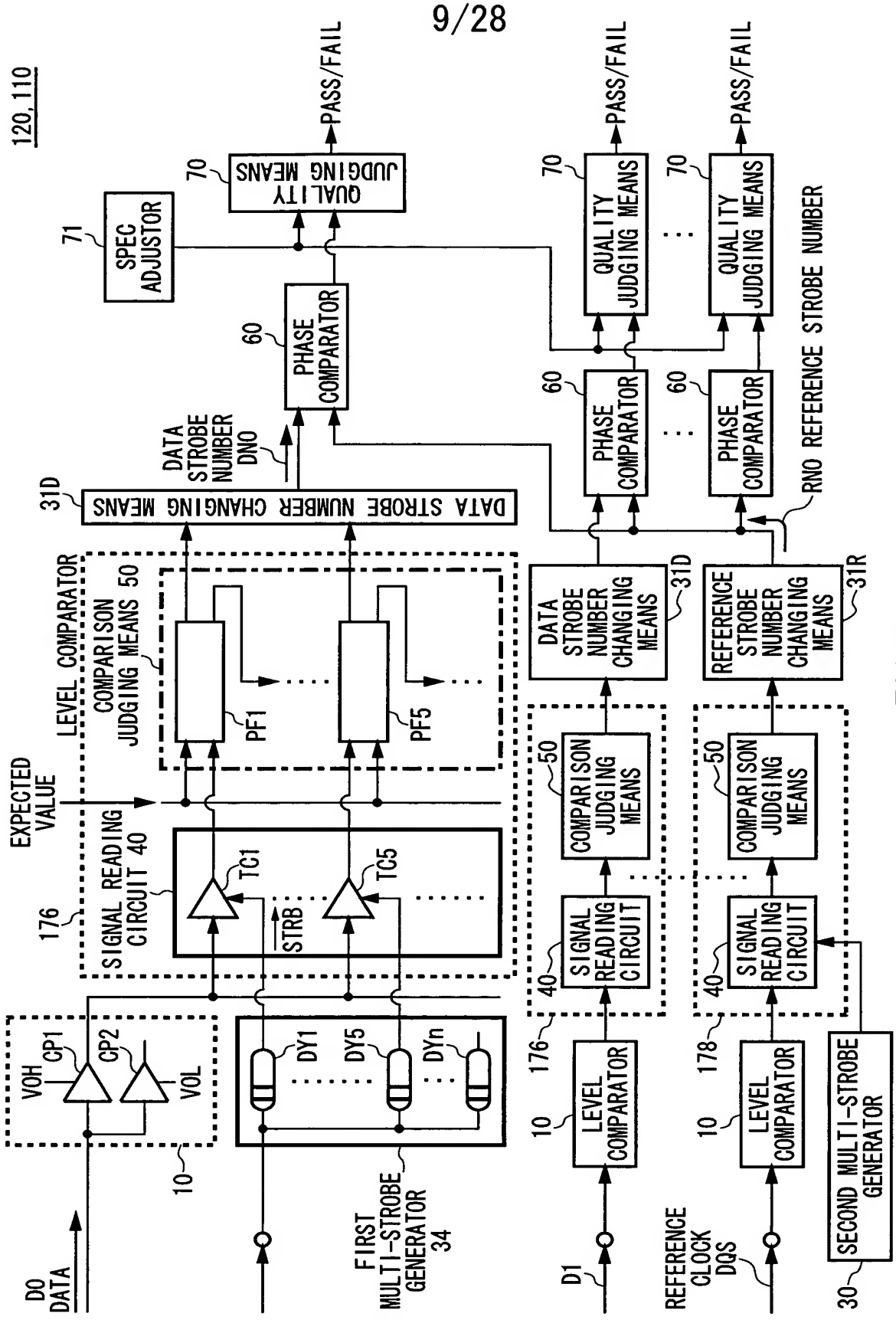
120, 110
PASS/FAIL
70
QUALITY JUDGING MEANS
71
SPEC ADJUSTOR
60
PHASE COMPARATOR
DATA STROBE NUMBER DNO
31D
DATA STROBE NUMBER CHANGING MEANS
LEVEL COMPARATOR
COMPARISON JUDGING MEANS 50
PF1
PF5
EXPECTED VALUE
SIGNAL READING CIRCUIT 40
176
TC1
TC5
STRB
VOH
CP1
CP2
VOL
10
DY1
DY5
DYn
FIRST MULTI-STROBE GENERATOR 34
D0 DATA
QUALITY JUDGING MEANS
PHASE COMPARATOR
RNO REFERENCE STROBE NUMBER
DATA STROBE NUMBER CHANGING MEANS
31D
REFERENCE STROBE NUMBER CHANGING MEANS
31R
COMPARISON JUDGING MEANS
50
SIGNAL READING CIRCUIT
40
LEVEL COMPARATOR
D1
178
REFERENCE CLOCK DQS
SECOND MULTI-STROBE GENERATOR
30

FIG. 9

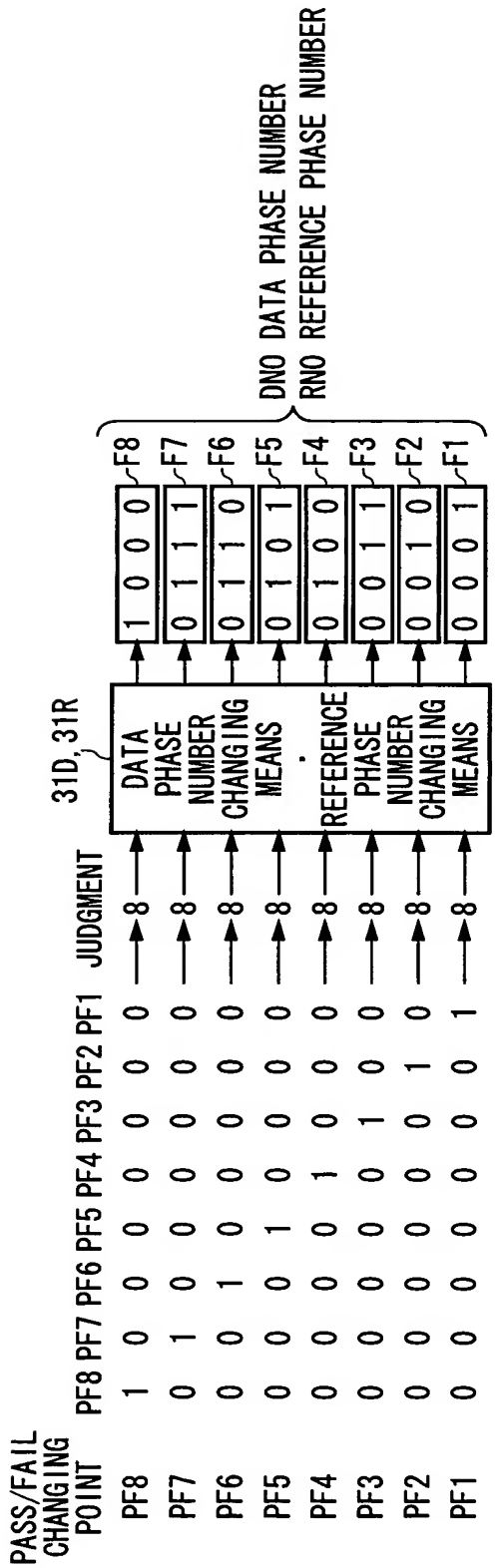
PASS/FAIL CHANGING POINT
PF8 PF7 PF6 PF5 PF4 PF3 PF2 PF1
PF8 1 0 0 0 0 0 0 0
PF7 0 1 0 0 0 0 0 0
PF6 0 0 1 0 0 0 0 0
PF5 0 0 0 1 0 0 0 0
PF4 0 0 0 0 1 0 0 0
PF3 0 0 0 0 0 1 0 0
PF2 0 0 0 0 0 0 1 0
PF1 0 0 0 0 0 0 0 1
JUDGMENT
8
31D, 31R
DATA PHASE NUMBER CHANGING MEANS
REFERENCE PHASE NUMBER CHANGING MEANS
DNO DATA PHASE NUMBER
RNO REFERENCE PHASE NUMBER
F8 1 0 0 0
F7 0 1 1 1
F6 0 1 1 0
F5 0 1 0 1
F4 0 1 0 0
F3 0 0 1 1
F2 0 0 1 0
F1 0 0 0 1

FIG. 10

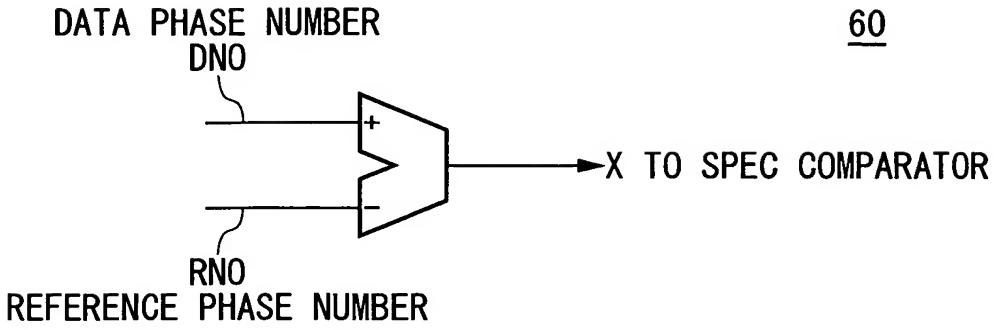
DATA PHASE NUMBER
DNO
60
+
-
X TO SPEC COMPARATOR
RNO
REFERENCE PHASE NUMBER

FIG. 11

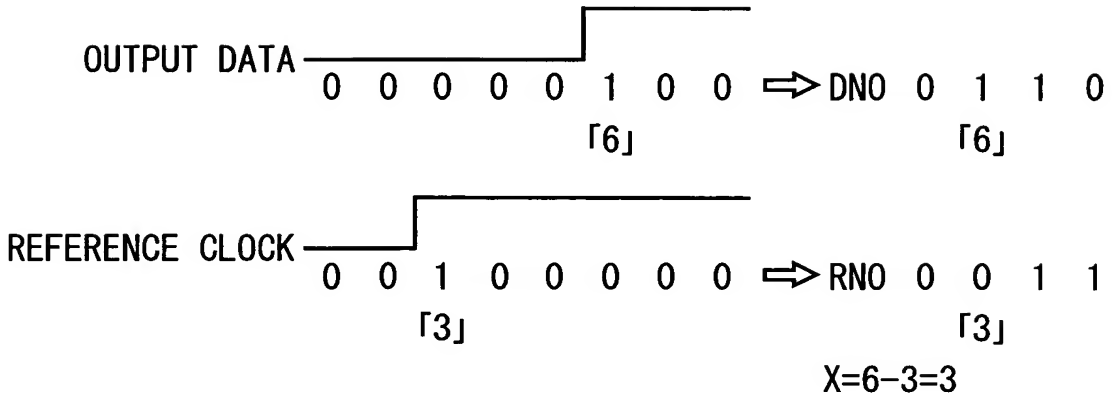
OUTPUT DATA
0 0 0 0 0 1 0 0
⇨DNO 0 1 1 0
「6」
「6」
REFERENCE CLOCK
0 0 1 0 0 0 0 0
⇨RNO 0 0 1 1
「3」
「3」
X=6-3=3

FIG. 12

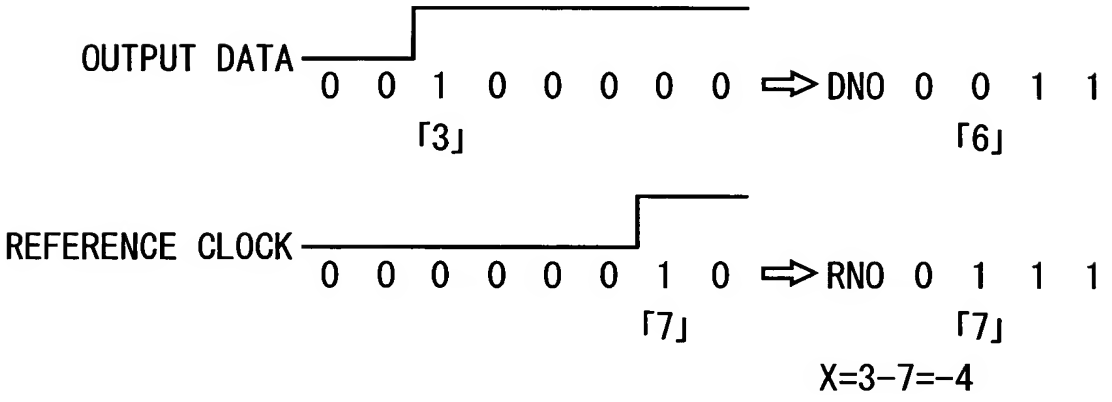
OUTPUT DATA
0 0 1 0 0 0 0 0
⇨DNO 0 0 1 1
「3」
「6」
REFERENCE CLOCK
0 0 0 0 0 0 1 0
⇨RNO 0 1 1 1
「7」
「7」
X=3-7=-4

FIG. 13

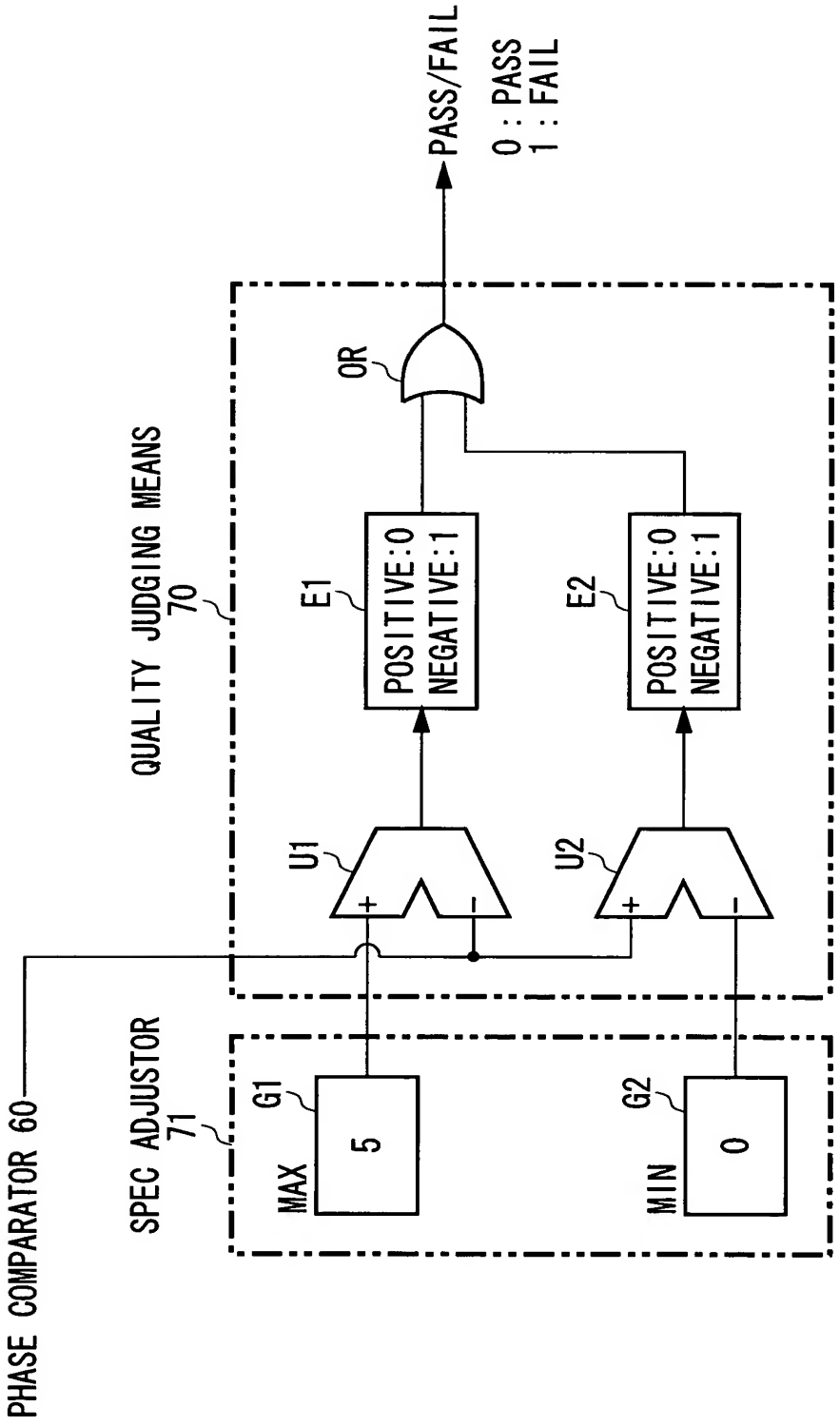
PHASE COMPARATOR 60
SPEC ADJUSTOR
71
G1
MAX
5
G2
MIN
0
QUALITY JUDGING MEANS
70
U1
U2
+
-
E1
POSITIVE:0
NEGATIVE:1
E2
POSITIVE:0
NEGATIVE:1
OR
PASS/FAIL
0 : PASS
1 : FAIL

FIG. 14

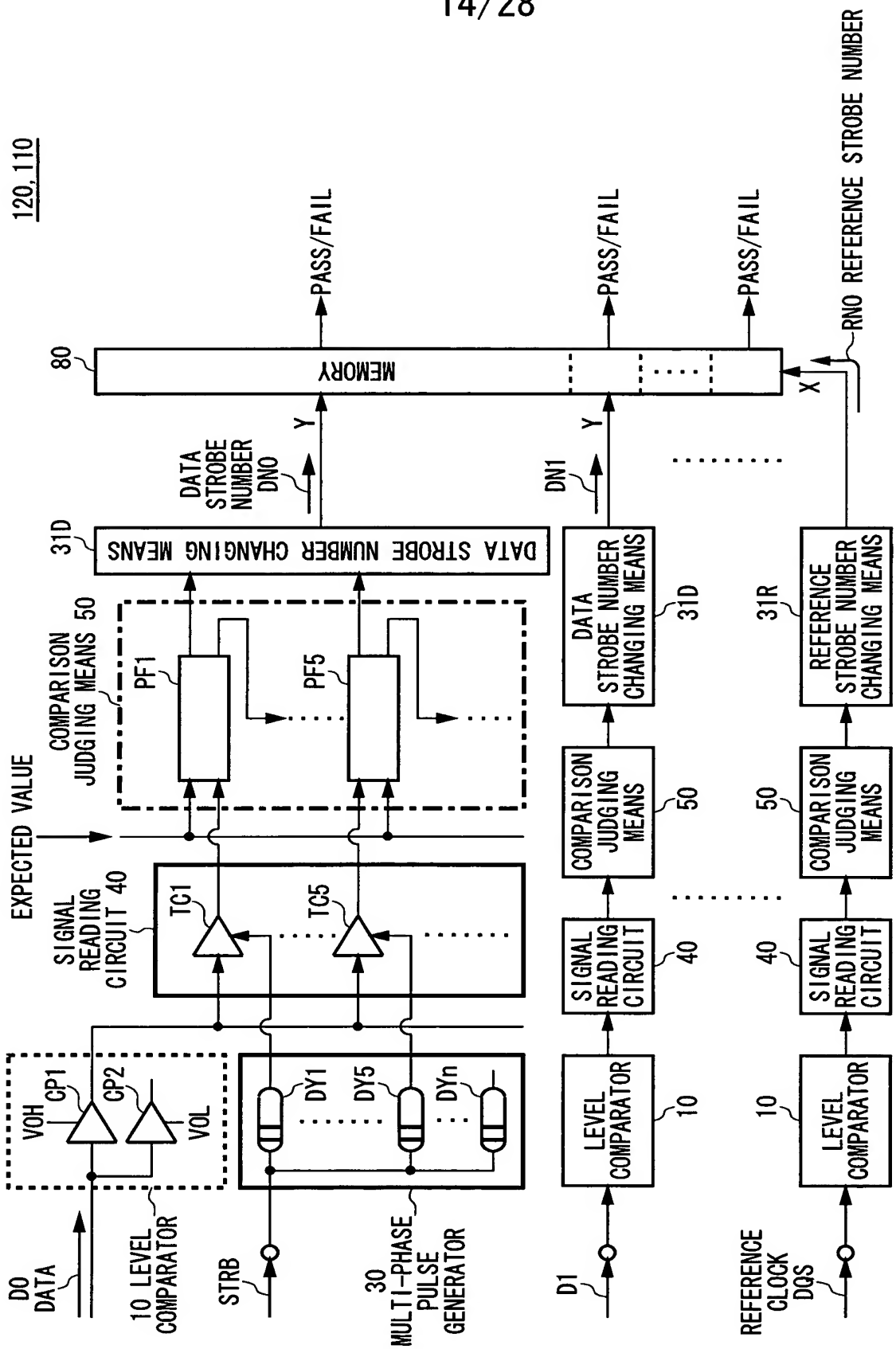
120,110
80
MEMORY
PASS/FAIL
PASS/FAIL
PASS/FAIL
RNO REFERENCE STROBE NUMBER
X
Y
Y
DATA STROBE NUMBER DNO
DN1
31D
DATA STROBE NUMBER CHANGING MEANS
DATA STROBE NUMBER CHANGING MEANS
31D
REFERENCE STROBE NUMBER CHANGING MEANS
31R
COMPARISON JUDGING MEANS 50
PF1
PF5
EXPECTED VALUE
SIGNAL READING CIRCUIT 40
TC1
TC5
COMPARISON JUDGING MEANS
50
COMPARISON JUDGING MEANS
50
SIGNAL READING CIRCUIT
40
SIGNAL READING CIRCUIT
40
VOH
CP1
CP2
VOL
DY1
DY5
DYn
LEVEL COMPARATOR
10
LEVEL COMPARATOR
10
DO DATA
10 LEVEL COMPARATOR
STRB
30 MULTI-PHASE PULSE GENERATOR
D1
REFERENCE CLOCK DQS

FIG. 15

DNO

DATA STROBE NUMBER

8	7	6	5	4	3	2	1	0
7	6	5	4	3	2	1	0	−1
6	5	4	3	2	1	0	−1	−2
5	4	3	2	1	0	−1	−2	−3
4	3	2	1	0	−1	−2	−3	−4
3	2	1	0	−1	−2	−3	−4	−5
2	1	0	−1	−2	−3	−4	−5	−6
1	0	−1	−2	−3	−4	−5	−6	−7
	1	2	3	4	5	6	7	8

RNO REFERENCE STROBE NUMBER

FIG. 16A

DNO

DATA STROBE NUMBER

8	F	F	F	F	F	P	P	P
7	F	F	F	F	P	P	P	P
6	F	F	F	P	P	P	P	P
5	F	F	P	P	P	P	P	F
4	F	P	P	P	P	P	F	F
3	P	P	P	P	P	F	F	F
2	P	P	P	P	F	F	F	F
1	P	P	P	F	F	F	F	F
	1	2	3	4	5	6	7	8

RNO REFERENCE STROBE NUMBER

FIG. 16B

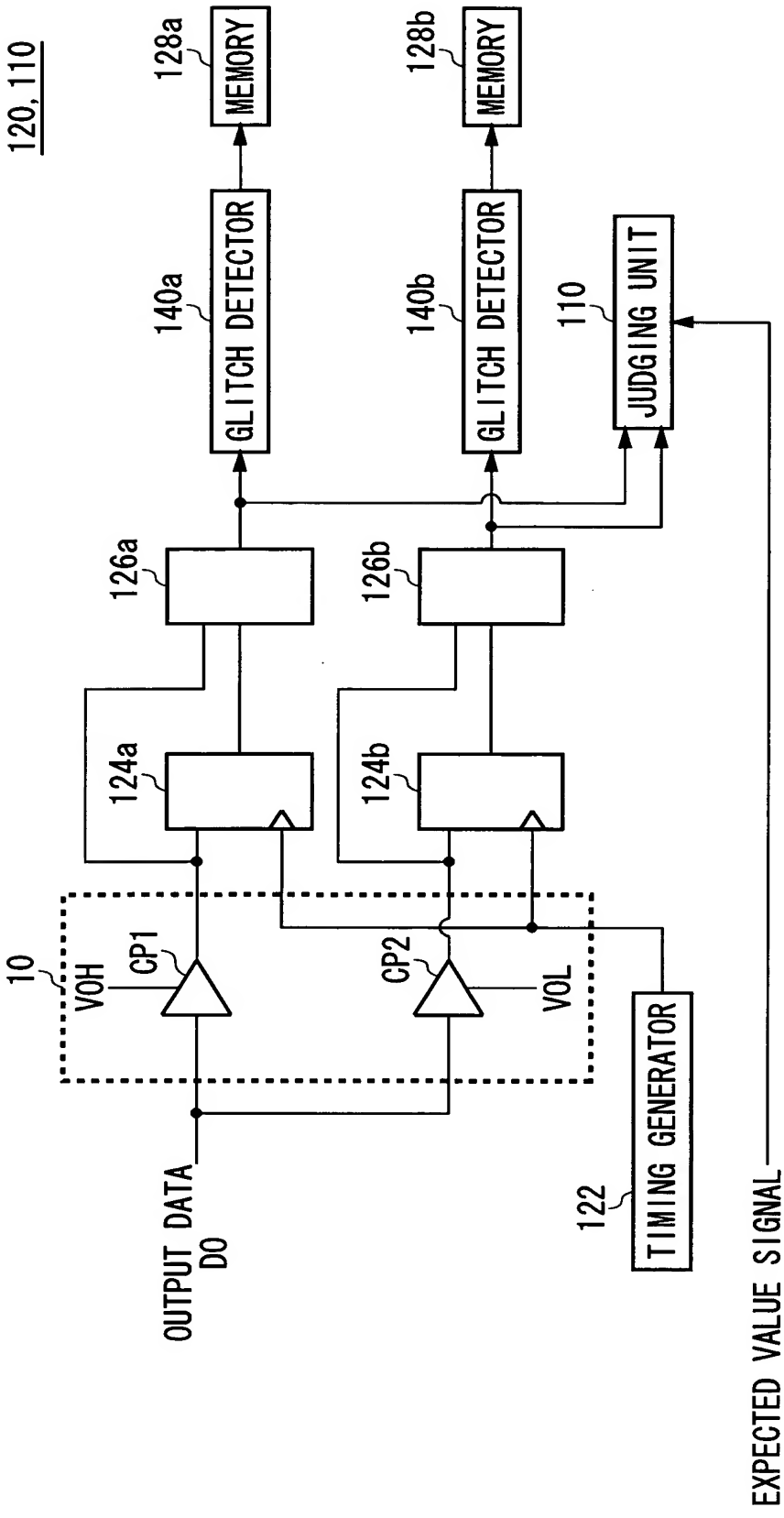
120, 110
128a
MEMORY
128b
MEMORY
140a
GLITCH DETECTOR
140b
GLITCH DETECTOR
110
JUDGING UNIT
126a
126b
124a
124b
10
VOH
CP1
CP2
VOL
OUTPUT DATA
DO
122
TIMING GENERATOR
EXPECTED VALUE SIGNAL

FIG. 17

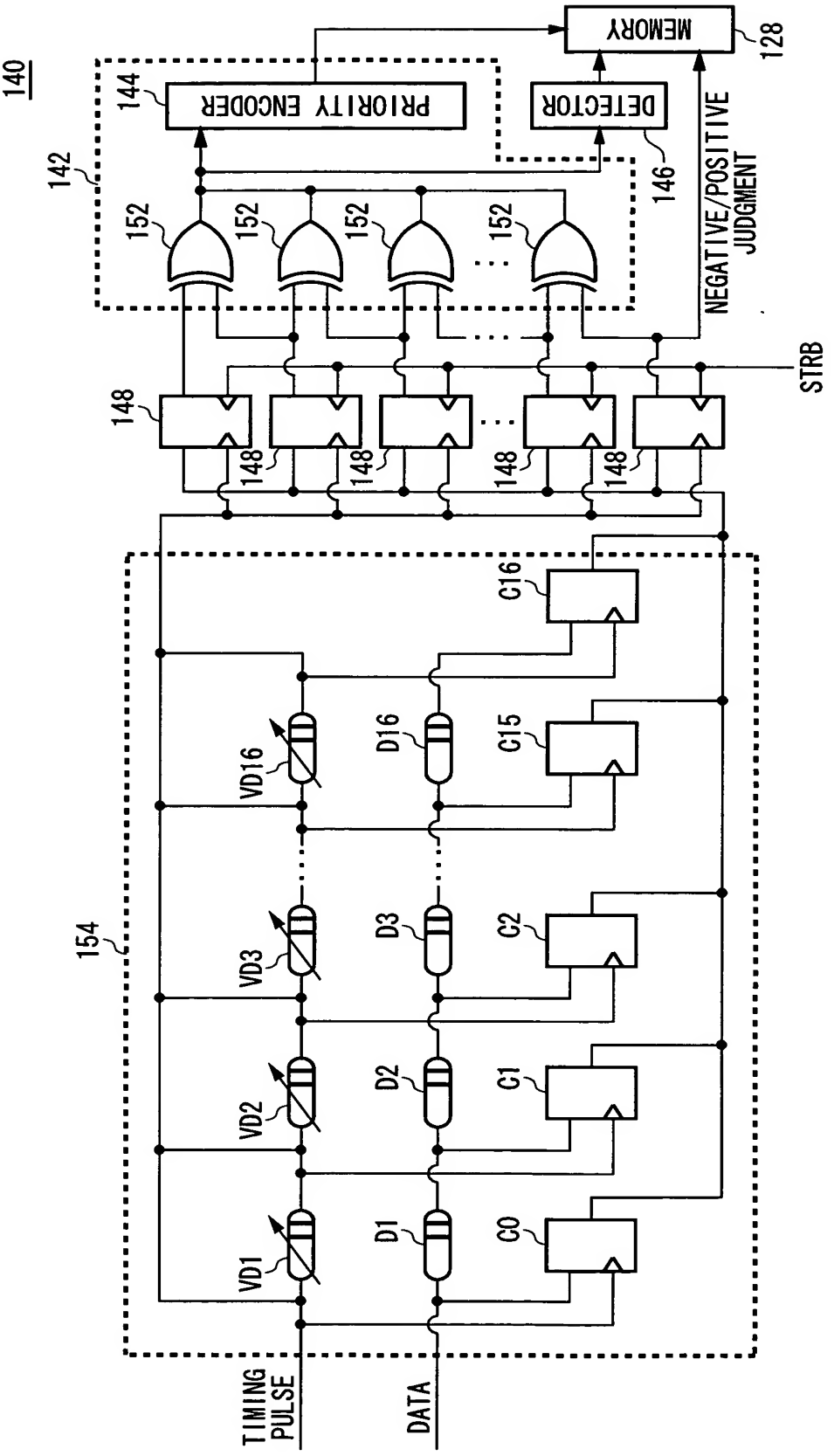
140
142
144
PRIORITY ENCODER
DETECTOR
MEMORY
128
146
NEGATIVE/POSITIVE JUDGMENT
152
148
STRB
154
C16
C15
C2
C1
C0
D16
D3
D2
D1
VD16
VD3
VD2
VD1
TIMING PULSE
DATA

FIG. 18

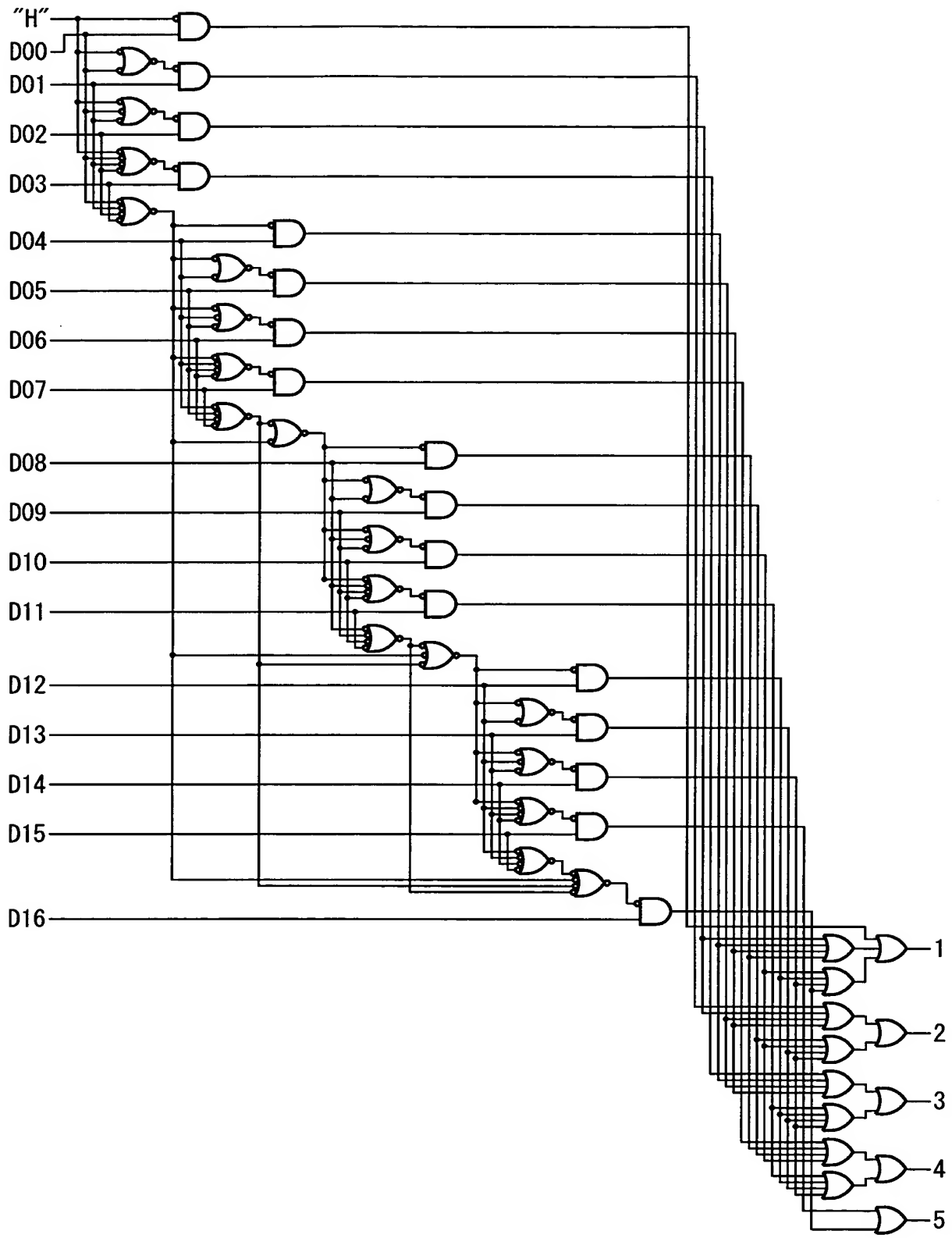
"H"
D00
D01
D02
D03
D04
D05
D06
D07
D08
D09
D10
D11
D12
D13
D14
D15
D16
1
2
3
4
5

FIG. 19

D16	D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	00000
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	00001
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	0	00010
X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	0	0	00011
X	X	X	X	X	X	X	X	X	X	X	X	X	1	0	0	0	00100
X	X	X	X	X	X	X	X	X	X	X	X	1	0	0	0	0	00101
X	X	X	X	X	X	X	X	X	X	X	1	0	0	0	0	0	00110
X	X	X	X	X	X	X	X	X	X	1	0	0	0	0	0	0	00111
X	X	X	X	X	X	X	X	X	1	0	0	0	0	0	0	0	01000
X	X	X	X	X	X	X	X	1	0	0	0	0	0	0	0	0	01001
X	X	X	X	X	X	X	1	0	0	0	0	0	0	0	0	0	01010
X	X	X	X	X	X	1	0	0	0	0	0	0	0	0	0	0	01011
X	X	X	X	X	1	0	0	0	0	0	0	0	0	0	0	0	01100
X	X	X	X	1	0	0	0	0	0	0	0	0	0	0	0	0	01101
X	X	X	1	0	0	0	0	0	0	0	0	0	0	0	0	0	01110
X	X	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	01111
X	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	10000
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	10001

FIG. 20

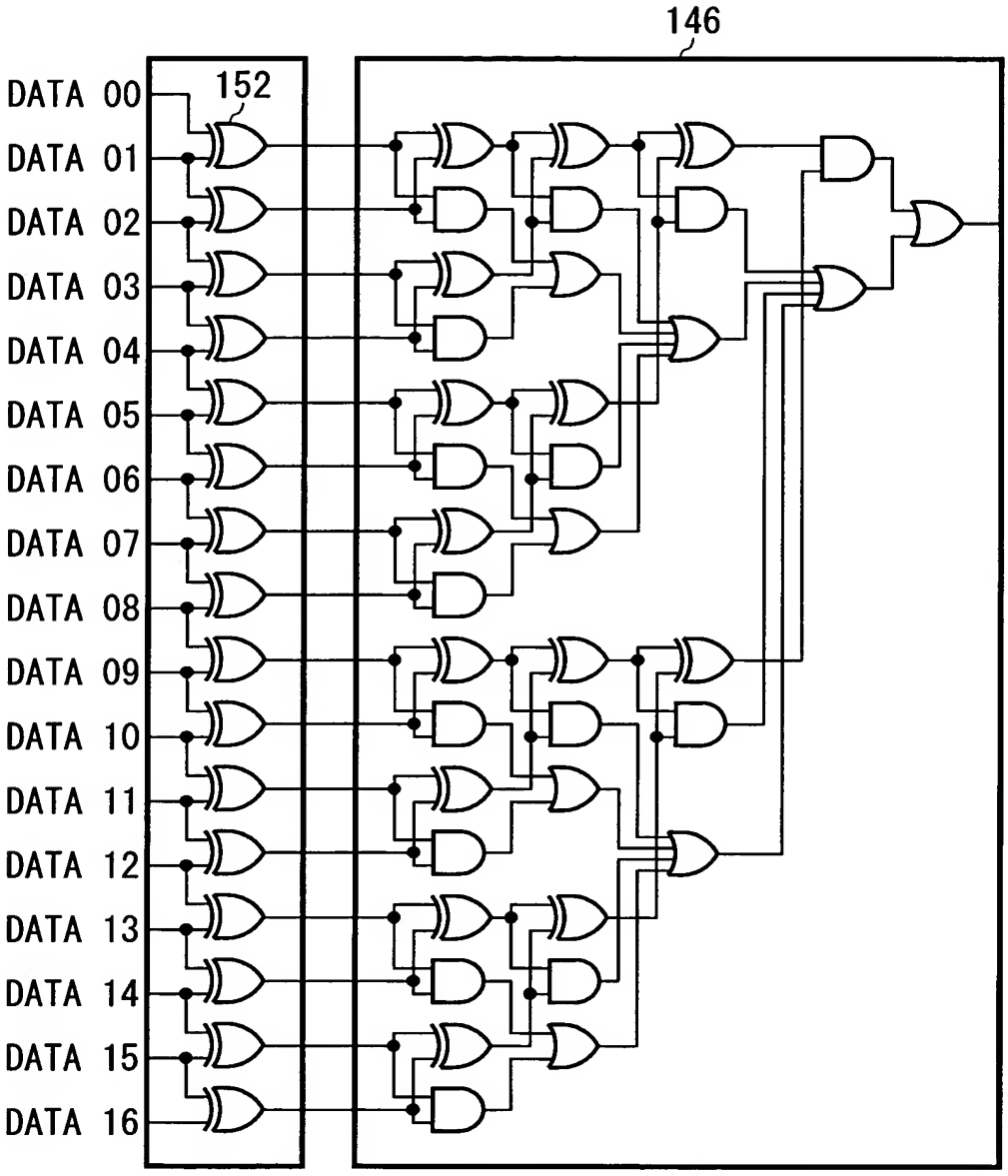
146
152
DATA 00
DATA 01
DATA 02
DATA 03
DATA 04
DATA 05
DATA 06
DATA 07
DATA 08
DATA 09
DATA 10
DATA 11
DATA 12
DATA 13
DATA 14
DATA 15
DATA 16

FIG. 21

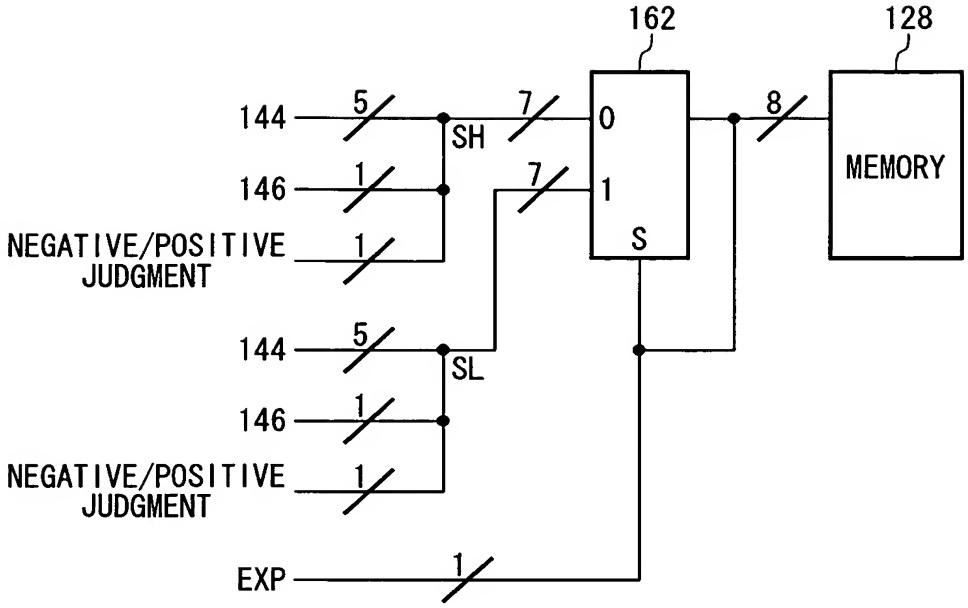

FIG. 22A

D7	D6	D5	D4	D3	D2	D1	D0
EXP	GLITCH DETECTION	NEGATIVE/POSITIVE JUDGMENT	CHANGING POINT CODE				

D0～D4 : CHANGING POINT CODE
#0 NONE OF CHANGING POINT
#1～#F CHANGING POINT WAS DETECTED
AT PHASE OF CHANGING POINT (VALUE-1) × 50PS
D5 : NEGATIVE/POSITIVE JUDGMENT
FALLING OF SH/SL WAS DETECTED IN CASE OF 1
RISING OF SH/SL WAS DETECTED IN CASE OF 0
D6 : GLITCH DETECTION
GLITCH WAS DETECTED IN CASE OF 1
GLITCH WAS NOT DETECTED IN CASE OF 0
D7 : EXP
FH IS MEMORIZED IN "H-LEVEL" EXPECTATION IN CASE OF 1
FL IS MEMORIZED IN "L-LEVEL" EXPECTATION IN CASE OF 0

FIG. 22B

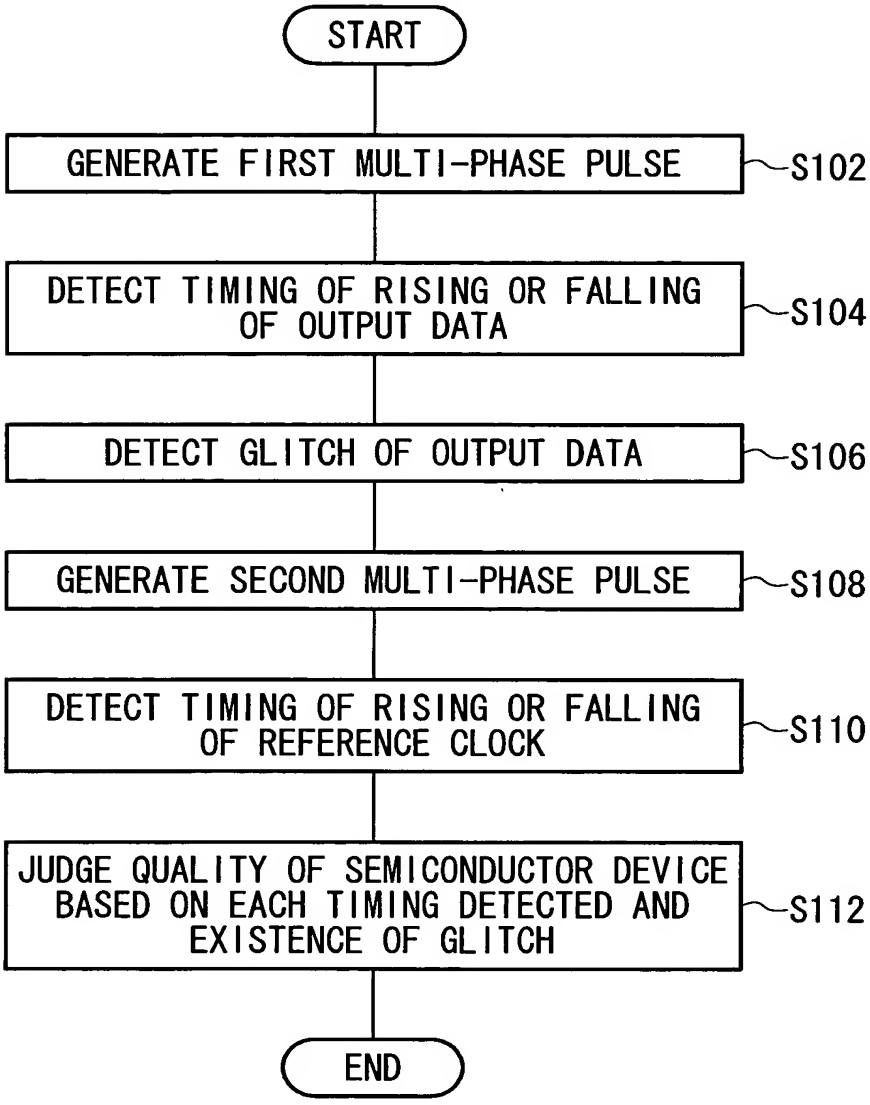
START
GENERATE FIRST MULTI-PHASE PULSE
S102
DETECT TIMING OF RISING OR FALLING OF OUTPUT DATA
S104
DETECT GLITCH OF OUTPUT DATA
S106
GENERATE SECOND MULTI-PHASE PULSE
S108
DETECT TIMING OF RISING OR FALLING OF REFERENCE CLOCK
S110
JUDGE QUALITY OF SEMICONDUCTOR DEVICE BASED ON EACH TIMING DETECTED AND EXISTENCE OF GLITCH
S112
END

FIG. 23

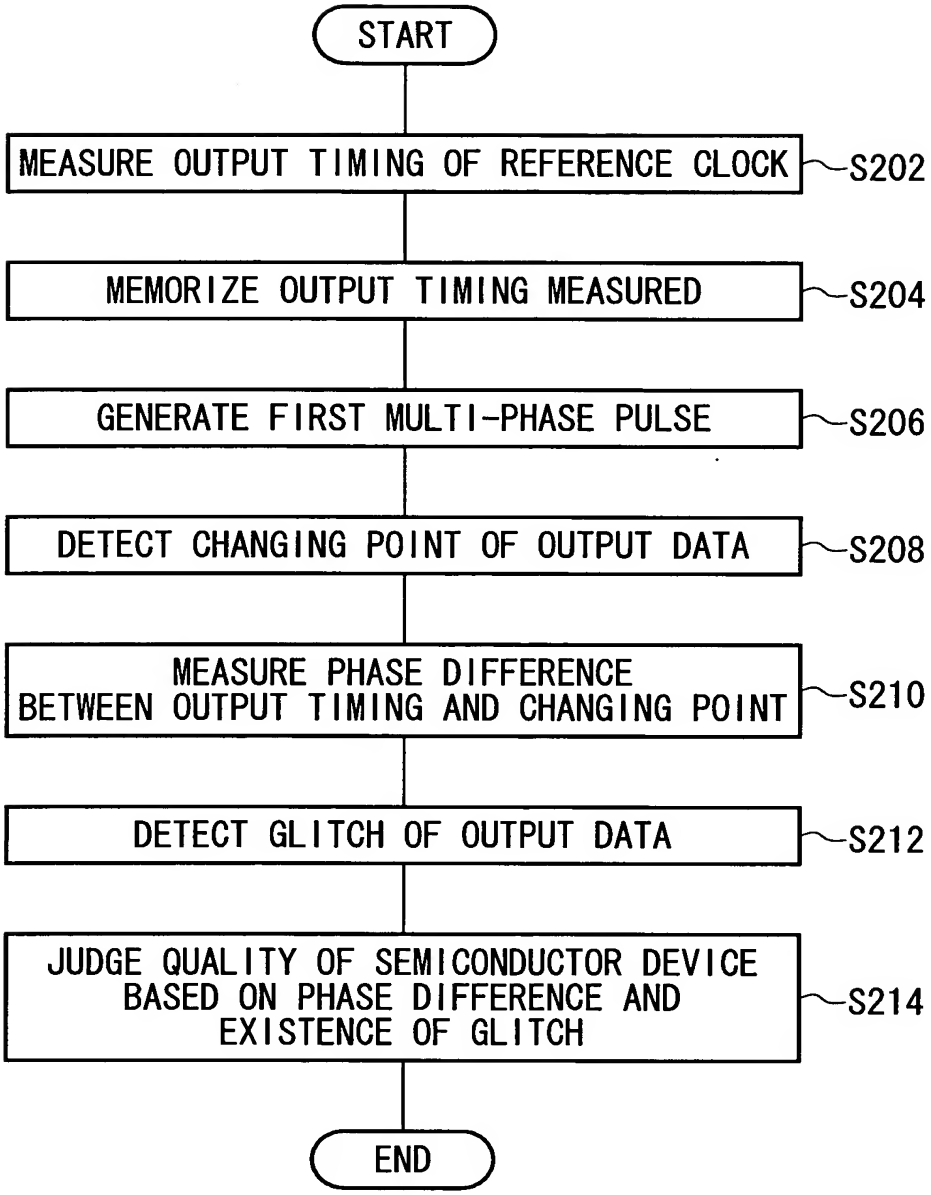
START
MEASURE OUTPUT TIMING OF REFERENCE CLOCK
S202
MEMORIZE OUTPUT TIMING MEASURED
S204
GENERATE FIRST MULTI-PHASE PULSE
S206
DETECT CHANGING POINT OF OUTPUT DATA
S208
MEASURE PHASE DIFFERENCE BETWEEN OUTPUT TIMING AND CHANGING POINT
S210
DETECT GLITCH OF OUTPUT DATA
S212
JUDGE QUALITY OF SEMICONDUCTOR DEVICE BASED ON PHASE DIFFERENCE AND EXISTENCE OF GLITCH
S214
END

FIG. 24

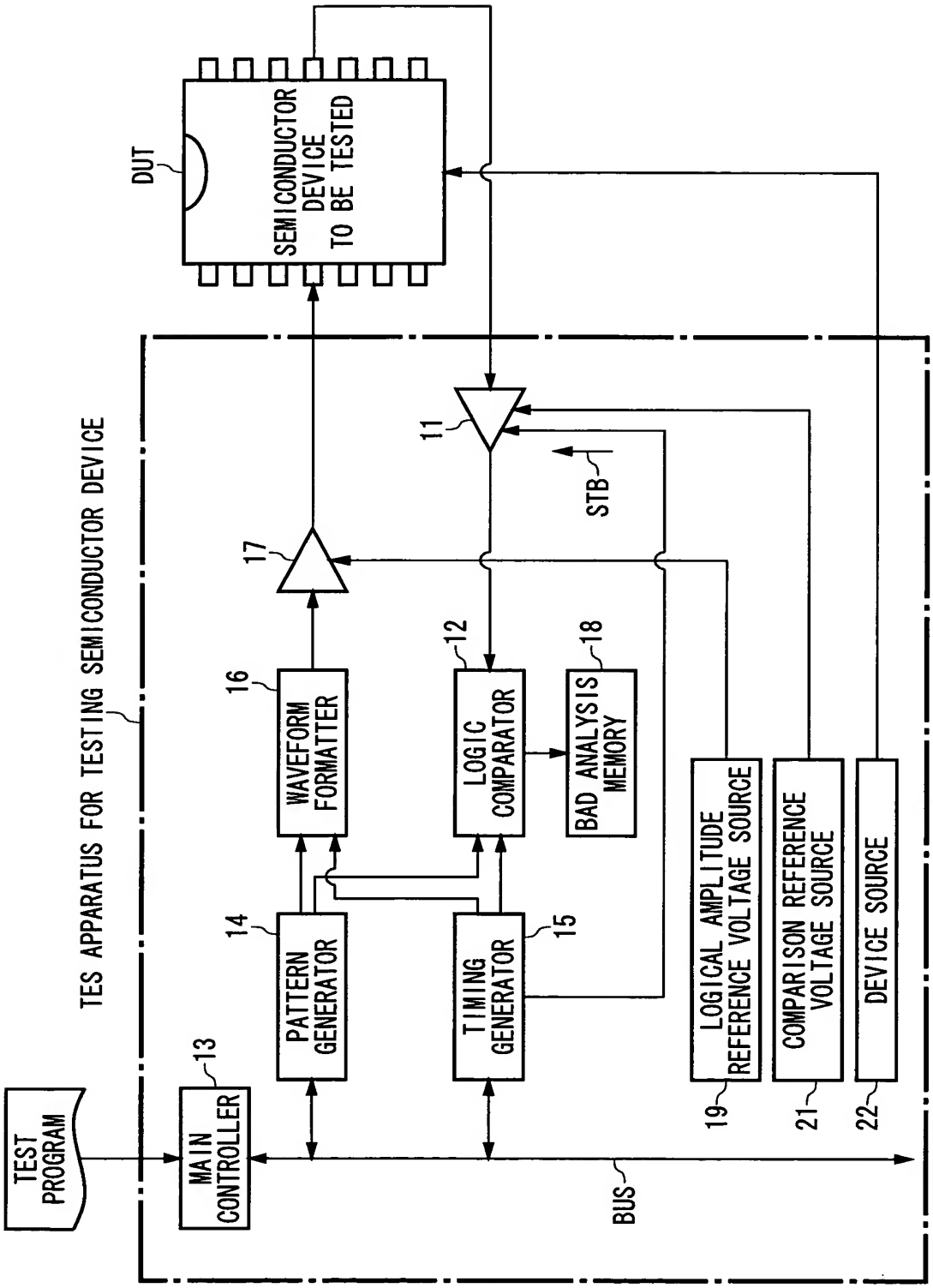
DUT
SEMICONDUCTOR DEVICE TO BE TESTED
TES APPARATUS FOR TESTING SEMICONDUCTOR DEVICE
11
STB
17
16
WAVEFORM FORMATTER
12
LOGIC COMPARATOR
18
BAD ANALYSIS MEMORY
14
PATTERN GENERATOR
15
TIMING GENERATOR
LOGICAL AMPLITUDE REFERENCE VOLTAGE SOURCE
19
COMPARISON REFERENCE VOLTAGE SOURCE
21
DEVICE SOURCE
22
TEST PROGRAM
13
MAIN CONTROLLER
BUS

FIG. 25

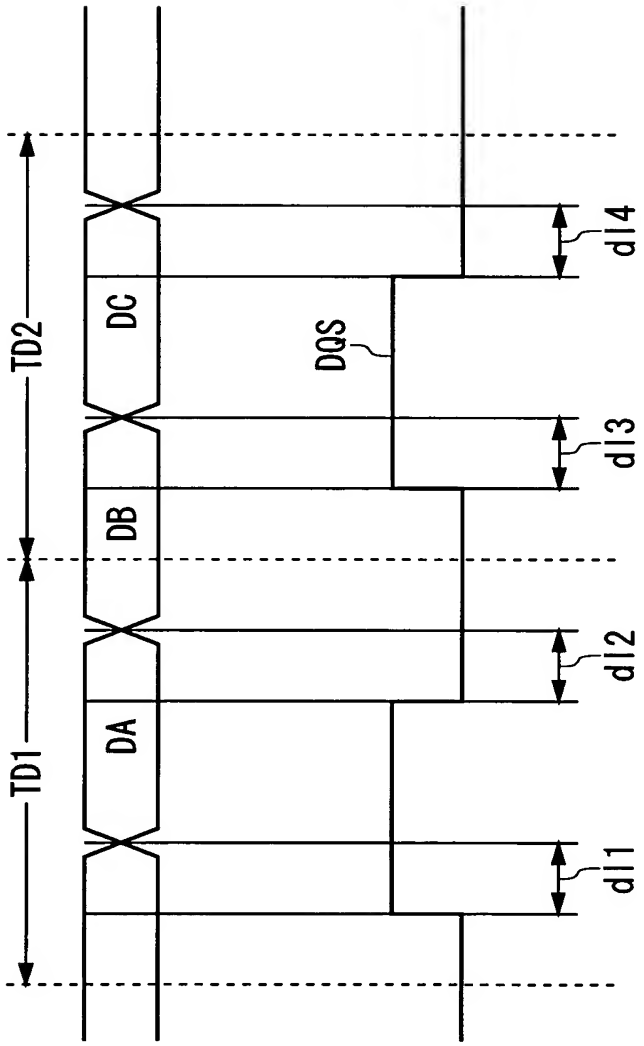

FIG. 26A

FIG. 26B

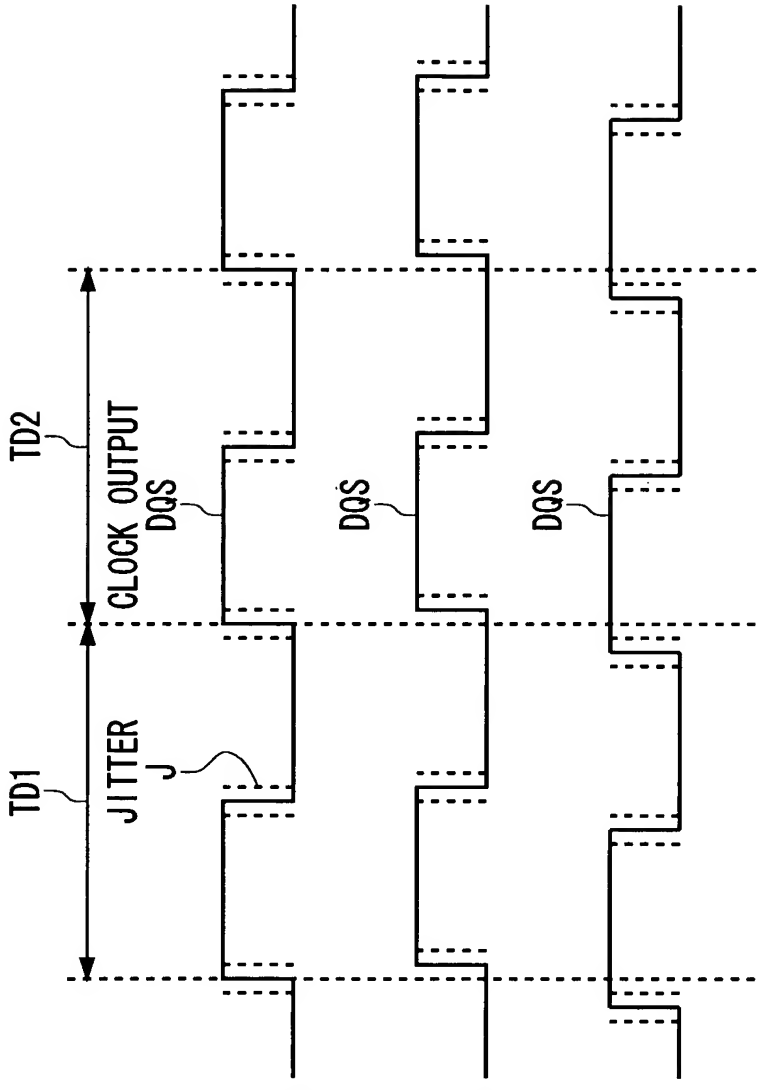

FIG. 27A

FIG. 27B

FIG. 27C

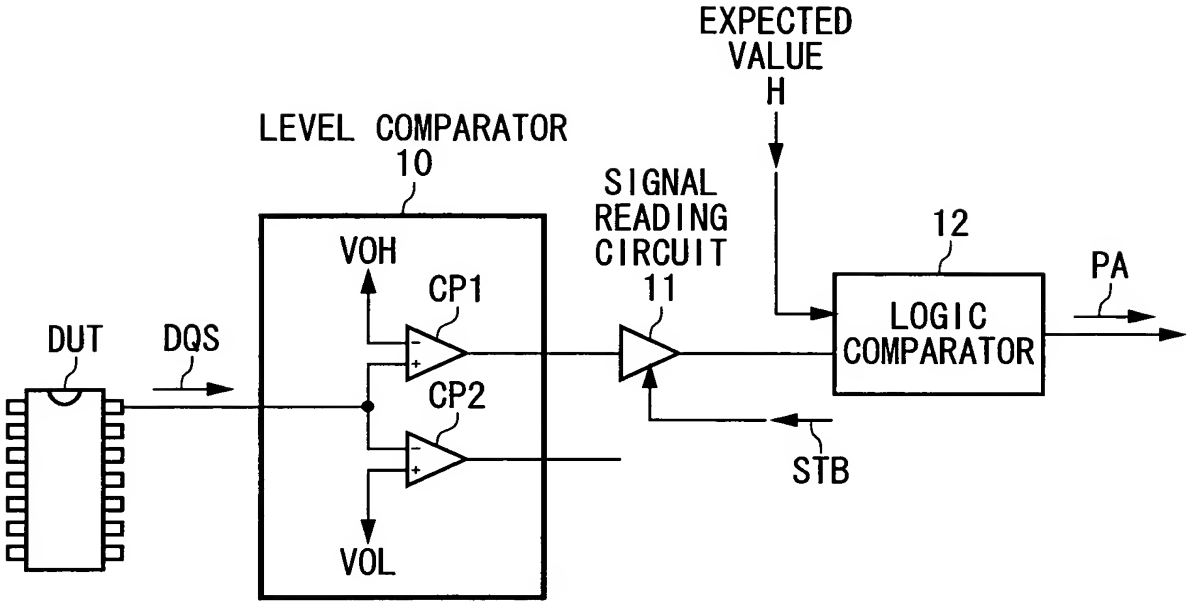
EXPECTED
VALUE
H
LEVEL COMPARATOR
10
SIGNAL
READING
CIRCUIT
11
12
PA
VOH
CP1
DUT
DQS
LOGIC
COMPARATOR
CP2
STB
VOL

FIG. 28

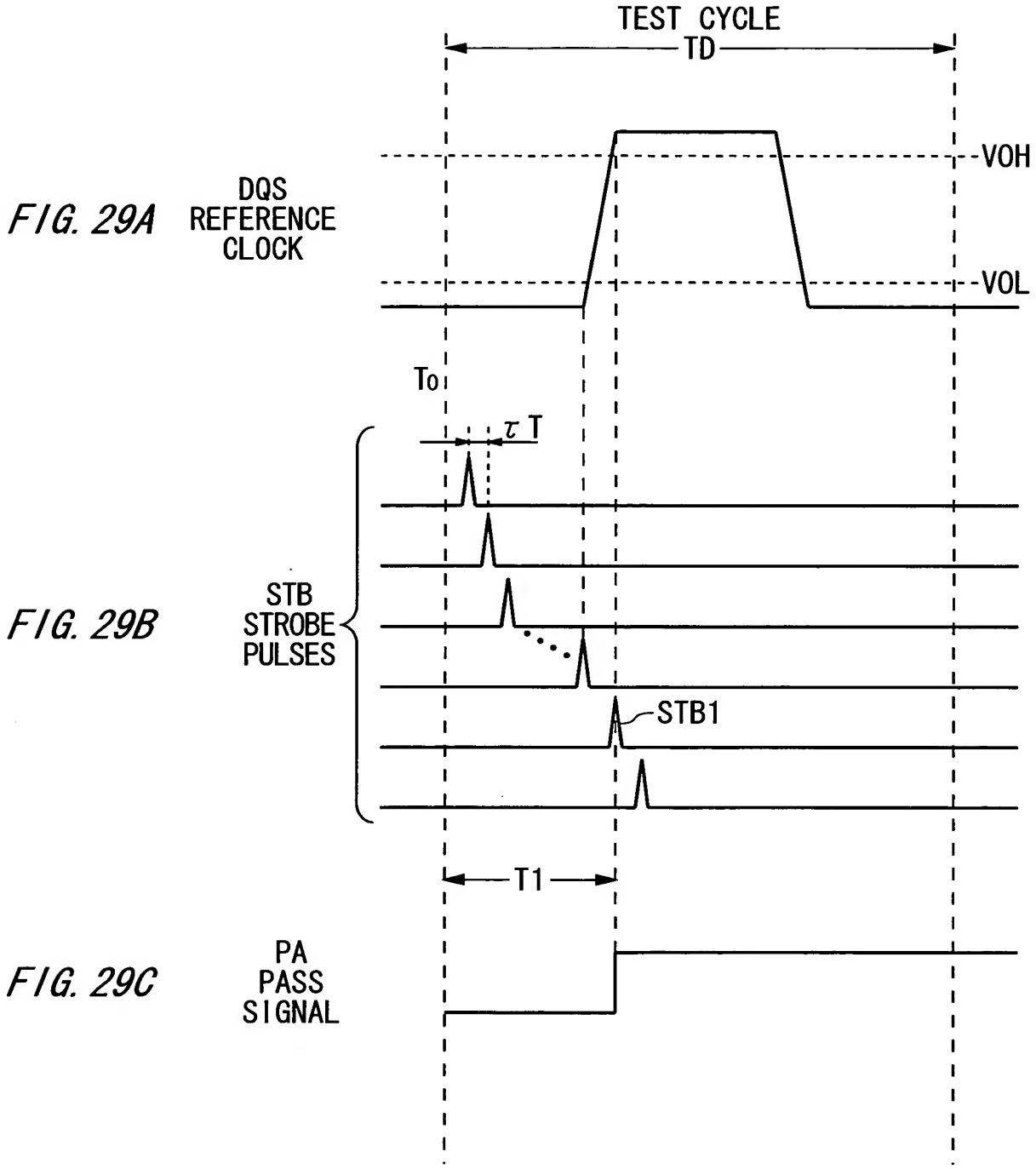

FIG. 29A

FIG. 29B

FIG. 29C